WHAT IS CLAIMED IS:

1. A method of digital circuit development comprising:

processing a description of the circuit in a computer system to generate electrical signals representative of a data model including information on logical parameters of the circuit and information on physical parameters of the circuit;

causing the computer system to use the data model to synthesize logic elements in accordance with the logical parameters therein; and

causing the computer system to use the data model to generate physical placement information for the logic elements in accordance with the physical parameters therein.

2. The method of claim 1, wherein the description is in a hardware description language.

3. The method of claim 1, wherein the data model is a hierarchy of data objects.

4. The method of claim 3, wherein:

the hierarchy includes at least one library object which owns an entity object;

the entity object owns at least one model object; and

the model object is a functional representation of the circuit.

5. The method of claim 4, wherein:

the hierarchy includes a plurality of library objects;

at least one of the plurality of library object is a technology library object; and

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at least one of the plurality of library objects is a target library object.

6. The method of claim 4, wherein:

the entity object owns a plurality of model objects;

each of the model objects is a different representation of the circuit; and

the model objects are functionally equivalent to one another.

7. The method of claim 4, wherein the at least one model object is implemented as a KD tree.

8. The method of claim 1, wherein the data model includes a representation of the circuit as a KD tree.

9. The method of claim 8, wherein each node of the KD tree corresponds to a physical attribute of a physical arrangement of the circuit.

10. The method of claim 9, wherein the physical attribute is a location of a portion of the circuit corresponding to the node within a chip.

11. The method of claim 9, wherein each node of the KD tree corresponds to a cutline of a semiconductor chip.

12. The method of claim 11, wherein at least one node of the KD tree has a cell associated therewith.

13. The method of claim 11, wherein at least one node of the KD tree has two child nodes, the child nodes corresponding to portions of the circuit on opposite sides of the cutline.

14. The method of claim 1, wherein:

the data model includes a plurality of cells, each cell corresponding to a portion of the circuit;

the logical parameters include functionality of the cells; and

the physical parameters include at least one of physical area and physical placement of the cell.

15. The method of claim 14, wherein:

the physical parameters include physical placement of the cell; and

processing the circuit description includes a step of assigning arbitrary physical placement parameters to the cells.

16. The method of claim 15, wherein causing the computer system to generate physical placement information includes causing the computer to modify the arbitrary physical placement parameters.

17. The method of claim 1, further comprising the step of using a common tool to evaluate the logical information and to evaluate the physical placement information.

18. The method of claim 17, wherein the common tool is a timing simulator.

19. The method of claim 1, further comprising:

storing the data model in the computer system;

specifying a physical area of the circuit less than the entire circuit area; and

retrieving a portion of the data model corresponding to the physical area while not retrieving portions of the data model not corresponding to the physical area.

20. The method of claim 1, further comprising:

making a copy of the data model; and

using the copy to formally validate the circuit.

21. A computer-readable medium storing a data structure for representing digital circuits, wherein:

the data structure includes a root containing at least one library;

each library contains at least one entity;

each entity contains at least one model and at least one port;

each model contains at least one cell, at least one net and at least one pin; and

each cell contains at least one pin.

22. The computer-readable medium of claim 21, wherein the data structure includes both logical synthesis information and physical placement information.

23. The computer-readable medium of claim 21, wherein the library includes a technology library and a circuit library.

24. The computer-readable medium of claim 21, wherein each entity is representative of a circuit.

25. The computer-readable medium of claim 24, wherein each model is representative of an implementation of the circuit represented by the entity which contains the model.

26. The computer-readable medium of claim 25, wherein:

at least one entity contains a plurality of models; and

the plurality of models are each representative of a different implementation of the circuit represented by the entity which contains the model.

27. The computer-readable medium of claim 21, comprising:

a plurality of cells;

wherein at least one of the plurality of cells is a primitive cell, and

at least one of the plurality of cells is a non-primitive cell.

28. The computer-readable medium of claim 21, wherein each model is represented in the data structure as a KD tree.

29. The computer-readable medium of claim 28, wherein each non-terminal node of the KD tree corresponds to a core cutline.

30. The computer-readable medium of claim 29, wherein each of the non-terminal KD tree nodes includes cells touching its corresponding cutline.